CLAIMS

1. Circuitry for multiplying a first signed operand of a first bit width and a second signed operand of a second bit width, comprising:

recoding circuitry for receiving the first signed operand and the second signed operand and providing a plurality of intermediate partial products;

sign extension adjustment circuitry coupled to the second signed operand, the sign extension adjustment circuitry providing a sign extension adjustment term that is equal to a negative value of the second signed operand multiplied by two raised to a power of N, where N is equal to the first bit width of the first signed operand; and

adder circuitry coupled to the recoding circuitry and the sign extension adjustment circuitry for compressing the plurality of intermediate partial products and the sign extension adjustment term to provide a final product.

2. The circuitry of claim 1 wherein the recoding circuitry is a modified Booth's recoder.

3. The circuitry of claim 1 wherein the sign extension adjustment circuitry further comprises circuitry for forming a two's complement of the second signed operand and appending a zero bit value to a predetermined number of least significant bits of the two's complement.

4. The circuitry of claim 3 wherein the circuitry for forming is further characterized as being means for performing the two's complement by forming an inverse of the second signed operand and incrementing the inverse by one.

5. The circuitry of claim 3 wherein the circuitry for forming is further characterized as being means for:

performing the two's complement by forming an inverse of the second signed operand, appending ones to the predetermined number of least significant bits of the inverse, and coupling the inverse to the adder circuitry; and

wherein the adder circuitry is further characterized as having means for:

selectively adding one to the inverse when compressing the plurality of intermediate partial products.

6. The circuitry of claim 1 wherein the first bit width is equal to the second bit width.

7. The circuitry of claim 1 wherein the first bit width is different from the second bit width.

8. The circuitry of claim 1 wherein the adder circuitry further comprises:

a plurality of multiple input/two output carry save adders (CSAs) and a carry lookahead adder for providing the final product.

9. The circuitry of claim 6 wherein the multiple/input/two output carry save adders comprise a plurality of four/two and three/two carry save adders.

10. In an electronic circuit, a method for multiplying a first signed operand having a negative value and a second signed operand, comprising:

storing the first signed operand and the second signed operand in a storage circuit;

generating a plurality of partial products from the first signed operand and the second signed operand without sign extending the first signed operand;

generating a sign extension adjustment term by forming a value equal to a product of a negative of the second signed operand multiplied by 2^N, where N is equal to a bit width of the first signed operand;

compressing the plurality of partial products and the sign extension adjustment term to form an output product, the sign extension adjustment term correctly implementing sign extension of the first signed operand without delaying the generating of the plurality of partial products.

11. The method of claim 10 further comprising:

implementing a modified Booth's recoding of the second operand to reduce the plurality of intermediate partial products required.

12. The method of claim 10 further comprising:

generating the sign extension adjustment term by forming an inverse of the second signed operand;

appending ones to the predetermined number of least significant bits of the inverse; and

adding one to the inverse after the step of appending ones to the inverse.

13. The method of claim 10 further comprising:

generating the sign extension adjustment term by forming an inverse of the second signed operand;

appending ones to the predetermined number of least significant bits of the inverse; and

adding, when compressing the plurality of intermediate partial products, one to the inverse after the step of appending ones to the inverse.

14. The method of claim 10 wherein the plurality of partial products are generated in parallel with generating the sign extension adjustment term to improve processing time required to form the output product.

15. The method of claim 10 where generating the plurality of partial products is implementing with a plurality of carry save adders for generating a sum term and a carry term, and a carry look ahead adder for generating the output product from the sum term and the carry term.

16. The method of claim 10 further comprising:

determining whether generating the sign extension adjustment term is necessary by verifying that signed operands are being used, that the first signed operand has a negative value, and that the first signed operand has a bit width that is less than a predetermined register width.

17. A multiplier comprising:

a first register for receiving and storing a first operand;

a second register for receiving and storing a second operand;

a modified Booth's recoder coupled to the first register and the second register, the modified Booth's recoding performing a predetermined radix recoding of the second operand;

a plurality of carry save adders coupled to the modified Booth's recoder, the plurality of carry save adders forming a plurality of partial products, at least one of the plurality of carry save adders having an input for receiving a sign extension adjustment term; and

compensation circuitry having an input for receiving the second operand, and having an output coupled to the input of the at least one of the plurality of carry save adders, the compensation circuitry selectively generating the sign extension adjustment term by forming a value equal to a product of a negative of the second operand and 2^N, where N is equal to a bit width of the first operand, the compensation circuitry forming the sign extension adjustment term in parallel with the predetermined radix recoding of the second operand.

18. The multiplier of claim 17 wherein the compensation circuitry selectively generates the sign extension adjustment term only when the first operand is a negative signed operand.

19. The multiplier of claim 17 wherein the compensation circuitry further comprises:

a two's complement circuit for forming a two's complement of the second operand to obtain the negative of the second operand; and

logic circuitry for selectively appending bit values of zero to one or more predetermined partial products.

20. The multiplier of claim 19 wherein the two's complement circuit further comprises:

an inverter having an input for receiving the second operand and an output; and

an incrementer having an input coupled to the output of the inverter and an output for providing the output of the inverter incremented by one.